

Using Multiple Scales Method to calculate threshold crossing time for the ramp response for high inductance VLSI interconnects.

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Abstract

The paper presents a new method of deriving the closed form formula for the output voltage and threshold crossing time for low-loss on-chip upper layer interconnects. The threshold crossing time solution for the ramp excitation is derived. The calculation of output voltage of two coupled interconnects for the ramp input is also presented.

I. Introduction

Faster circuits and smaller die sizes means that influence of interconnect on device efficiency becomes more critical. Especially the long interconnects as signal and clock lines should be considered in simulation of VLSI devices, because of high impact in crosstalks and delays causing failures in the whole system [1]. Higher level interconnects due to their relatively long lengths are designed with larger cross sections to reduce losses. Then considering long lengths interconnects, we can talk about lower resistance per unit length. In on-chip interconnects that resistance is still high per unit length, but distances on chips are short enough to designate higher level interconnect as low-loss interconnects [1].

The analysis of the long on-chip interconnects requires the assumption of an appropriate model. Because of the relatively high inductance of the line and new low resistance materials, the RLC - line instead of RC - line model must be considered. Due to high inductance, the signal does not reach the steady state monotonically, but in an oscillatory way. Since the oscillations are related to the traveling wave reflections, and since in such cases the first traveling wave usually crosses the steady state level (ringing), it is sufficient to compute only the first wave to determine the threshold crossing times. For many cases it is not possible to assume that the signal input is a step voltage signal because of its rise time comparable to delay time. In such cases it is necessary to calculate the output signal for the ramp input modeling the real input

The paper is organized as follows: in Section II there is a multiple scales method presented in application to high inductance interconnect model. In the Section III we show how to extend calculations for ramp response of interconnect, In Section IV we present how to extend the solution for the single interconnect to the system of two coupled interconnects. In the Section V we the method of threshold crossing time calculation. The simulation results are shown in Section VI and the conclusions are presented in the last section.

II. The Multiple Scales Method

The multiple scales method is a perturbation method of calculating differential equations. We use this method to calculate the step response of the system of differential equation modeling the interconnect as a transmission RLC line (1). The ramp response we obtain after some simple mathematical transformations from the step response. The considered interconnect model is presented at Fig 1.

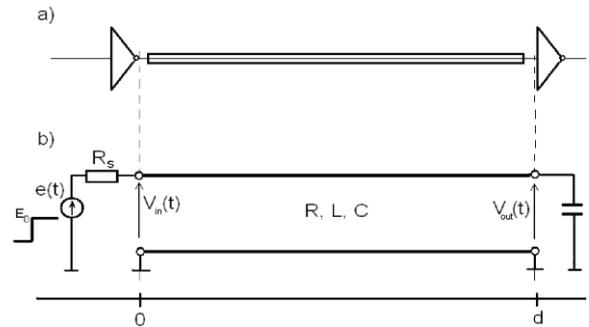


Fig. 1. a) The considered system inverter-interconnect-inverter, b) the model of the considered system

For such a system we can write the differential equation in the form:

$$\begin{cases} -\frac{\partial v}{\partial x} = Ri + L \frac{\partial i}{\partial t}, \\ -\frac{\partial i}{\partial x} = C \frac{\partial v}{\partial t} \end{cases} \quad (1)$$

with initial and boundary conditions

$$i(x,0) = 0, \quad v(x,0) = 0, \quad (2)$$

$$e(t) - R_s i(0, t) = v(0, t),$$

$$-i(d, t) = C_0 \frac{\partial v(d, t)}{\partial t}, \quad (3)$$

where

R, L, C – line parameters, C_0 – input inverter capacitance, R_s – output inverter resistance, $i(x,t), v(x,t)$ – current and voltage in line, respectively, d – line length, t, x – time and space variable, respectively.

In the perturbation methods there is a need to choose the perturbation parameter which values are relatively small. In our consideration we assume that, due to the line resistance in low resistance interconnects is small compared to the lossless line impedance Z_0 ($Z_0 > R_l$), the perturbation parameter:

$$\varepsilon = \sqrt{\frac{C_t}{L_t}} R_t = \frac{R_t}{Z_0} < 1 \quad (4)$$

where $R_t = R \cdot d$, $C_t = C \cdot d$, $L_t = L \cdot d$.

To simplify the calculation and enable the perturbation parameter occur in differential equation we are scaling variables occurring in system (1):

$$y = \frac{x}{d}, \quad \tau = \frac{t}{\sqrt{L_t C_t}}, \quad \tilde{v} = -\sqrt{\frac{C_t}{L_t}} v, \quad \tilde{e} = \sqrt{\frac{C_t}{L_t}} e, \quad \beta = \sqrt{\frac{C_t}{L_t}} R_s$$

and we can rewrite (2) and (3) in the following way

$$\begin{aligned} \frac{\partial \tilde{v}}{\partial y} &= \varepsilon i + \frac{\partial i}{\partial \tau}, \\ \frac{\partial i}{\partial y} &= \frac{\partial \tilde{v}}{\partial \tau}, \end{aligned} \quad (5)$$

$$\begin{aligned} \tilde{e}(\tau) - \beta i(0, \tau) &= -\tilde{v}(0, \tau), \\ -i(1, \tau) &= \frac{C_0}{C_t} \frac{\partial \tilde{v}(1, \tau)}{\partial \tau}. \end{aligned} \quad (6)$$

Generally, the multiple scales method [5] requires expansion of the solution for differential equations into a power series of ε . Additionally, new space variables are introduced. In our analysis we limit the expansion to two terms and two space variables. For the system of equations (5) we have

$$\begin{aligned} \tilde{v}(y, \tau) &= \tilde{v}_0(y_0, y_1, \tau) + \varepsilon \cdot \tilde{v}_1(y_0, y_1, \tau), \\ i(y, \tau) &= i_0(y_0, y_1, \tau) + \varepsilon \cdot i_1(y_0, y_1, \tau), \\ y_0 &= y, \quad y_1 = \varepsilon \cdot y. \end{aligned}$$

And we construct the new systems of differential equations[2]:

$$O(1) \quad \begin{aligned} \frac{\partial \tilde{V}_0}{\partial y_0} &= s I_0, \\ \frac{\partial I_0}{\partial y_0} &= s \tilde{V}_0 \end{aligned} \quad (7)$$

$$\begin{aligned} \tilde{E}(\tau) - \beta I_0(0, 0, s) &= -\tilde{V}_0(0, 0, s), \\ -\alpha I_0(1, \varepsilon, s) &= s \tilde{V}_0(1, \varepsilon, s), \\ \alpha &= \frac{C_t}{C_0}, \end{aligned} \quad (8)$$

$$O(\varepsilon) \quad \begin{aligned} \frac{\partial \tilde{V}_1}{\partial y_0} &= s I_1 + I_0 + \frac{\partial \tilde{V}_0}{\partial y_1}, \\ \frac{\partial I_1}{\partial y_0} &= s \tilde{V}_0 + \frac{\partial I_0}{\partial y_1} \end{aligned} \quad (9)$$

$$\begin{aligned} \beta I_1(0, 0, s) &= \tilde{V}_1(0, 0, s), \\ -\alpha I_1(1, \varepsilon, s) &= s \tilde{V}_1(1, \varepsilon, s). \end{aligned} \quad (10)$$

The way of calculating the step output response for such a system is presented in [2,3]. In the next paragraph we will show how to extend it to ramp excitation, and calculate the

threshold time. The output voltage signal for the step response for first traveling way takes the form [2]:

$$\begin{aligned} v_{out}(d, t) &= v_{01}(d, t) + v_{11}(d, t) = \\ &= \frac{E_0}{\beta + 1} \left(A \cdot \frac{(t-T)}{T} \cdot e^{-\frac{\alpha}{T}(t-T)} - B \cdot \left(1 - e^{-\frac{\alpha}{T}(t-T)} \right) \right) \cdot \mathbf{1}(t-T), \end{aligned} \quad (11)$$

$$\text{where } A = -\varepsilon \cdot \alpha \cdot e^{-1.5\varepsilon}, \quad B = \frac{\varepsilon}{2} e^{-0.5\varepsilon} (1 + e^{-\varepsilon}) - \frac{\beta\varepsilon}{\beta+1} - 2e^{-0.5\varepsilon}.$$

Formula (11) is valid for the time $0 < t < 3T$.

III. Extension to the ramp excitation

In the simulation of many on-chip interconnects we have to take into consideration the influence of the input voltage rise time T_r , since its value is comparable to the time delay of the interconnect.

We can express the ramp excitation as

$$v_{in}(t) = \frac{E_0}{T_r} t \cdot \mathbf{1}(t) - \frac{E_0}{T_r} (t - T_r) \cdot \mathbf{1}(t - T_r) \quad (12)$$

We must consider two cases – one for $0 < t < T_r$, and the other for $t > T_r$. Denoting the response to ramp excitation at the end of the interconnect as $v_{out}^r(t, d)$ and using

$$v_{out}^r(t, d) = \begin{cases} \int_0^t v_{out}(\tau, d\tau) d\tau & t \leq T_r \\ \int_{t-T_r}^t v_{out}(\tau - T_r, d\tau) d\tau & t \geq T_r \end{cases}$$

we have the final output voltage signal

$$\begin{aligned} v_{out}^r(t) &= \frac{E_0}{(\beta+1)T_r} \left[\begin{aligned} &k \left(1 - e^{-\frac{\alpha}{T}(t-T)} \right) \\ &-\frac{t-T}{T} \left(B + \frac{A}{\alpha} e^{-\frac{\alpha}{T}(t-T)} \right) \end{aligned} \right], \\ &\text{for } t-T \leq T_r \end{aligned} \quad (13)$$

$$\begin{aligned} v_{out}^r(t) &= \frac{E_0}{(\beta+1)T_r} \left[\begin{aligned} &\left(\left(\frac{t-T-T_r}{T\alpha} \right) A \right) e^{-\frac{\alpha}{T}(t-T_r-T)} \\ &+ k \\ &-\left(\frac{t-T}{T\alpha} A + k \right) e^{-\frac{\alpha}{T}(t-T)} - \frac{T_r}{T} B \end{aligned} \right], \\ &\text{for } t-T \geq T_r \end{aligned}$$

$$\text{where } k = \left(\frac{A}{\alpha^2} + \frac{B}{\alpha} \right).$$

The presented approach allows calculating the approximated ramp excitation response. During the simulation we noticed that some improvement could be obtained if the perturbation parameter is scaled to $\varepsilon' = 3/5 \cdot \varepsilon$. The comparison of the results from SPICE, from formula (13) and from the improvement of (13) are presented in section 5. The curve representing the signal calculated using the scaled perturbation parameter is almost identical with the curve obtained by the SPICE simulator.

IV. The coupled lines extension

The considered interconnect output voltage response presented in Section III can be easily extended to the symmetrical coupled interconnects structure presented in Fig.2. The structure can be modeled by the system of two coupled interconnects with RLC transmission line parameters (M and C_m denote mutual inductance and capacitance, respectively). We can decouple two identical coupled interconnects, getting two independent lines with parameters as follows: $R_1=R_2=R$, $L_1=L+M$, $L_2=L+M$, $C_1=C-C_m$, $C_2=C+C_m$, $e_1(t)=e_2(t)=e(t)$, $R_{w1/2}=R_w$, $C_{01/2}=C_0$.

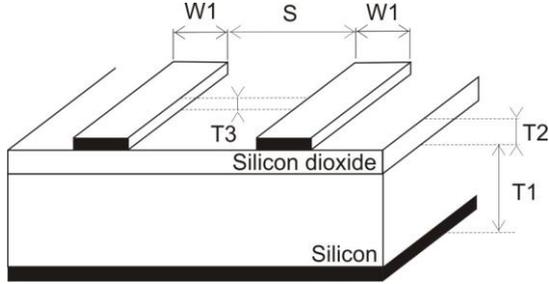


Fig. 2. The symmetrical coupled interconnect structure. Structure dimensions: $W_1=1\mu\text{m}$, $S=2\mu\text{m}$, $T_1=300\mu\text{m}$, $T_2=3\mu\text{m}$, $T_3=1\mu\text{m}$, length $d=5\text{mm}$, and the material parameters: $\epsilon_{\text{Si}}=11.9$, $\epsilon_{\text{SiO}_2}=4.2$, $\sigma_{\text{Si}}=10000[\text{S/m}]$ and $\sigma_{\text{Cu}}=2.73\text{e}+7[\text{S/m}]$.

After computing the ramp responses (13) for the two independent lines we can collect them in the following formulae for the end of the aggressor and victim line, respectively

$$v_{out}^a(t) = \frac{1}{2}(v_{c_1}(t) + v_{c_2}(t)), \quad v_{out}^v(t) = \frac{1}{2}(v_{c_1}(t) - v_{c_2}(t)) \quad (14)$$

where $v_{out}^a(t)$ and $v_{out}^v(t)$ denote the first traveling wave for the aggressor and victim line, respectively, and $v_{c_1}(t)$ and $v_{c_2}(t)$ denote the first traveling wave calculated from (13) for the first and second decoupled line, respectively. The application of the method is presented in Section VI.

V. The threshold crossing time

The computation of threshold crossing time is a challenge many authors try to deal with e.g. [4]. If we take into account the exact formula for the voltage ramp response expressed e.g. by (13) the problem during the ramp times ($t < T_r$) reduces to solving equation (15) with respect to t

$$\rho = \frac{E_0 k}{(\beta + 1) T_r} \left(1 - e^{-\alpha \frac{t-T}{T}} \right) - \frac{t-T}{T} \left(B + \frac{A}{\alpha} e^{-\alpha \frac{t-T}{T}} \right), \quad (15)$$

where ρ is the threshold value ($0 \div 1$). Equation (15) can be reduced to the form

$$z \cdot e^z = a, \quad (16)$$

where a is a constant, and z is the time function.

The left side of (16) is the function of z only and does not depend on the interconnect parameters (see Fig.3). Since the value of $z(t)$ is very small for the ramp excitation, we approximate the Lambert W function as

$$W(x) = 1/u_1 \cdot (\ln(x/u_0) - u_2) \quad (17)$$

where the approximation parameters u_0 and u_1 do not depend on interconnect RLC parameters and:

$$u_0 = -1.072, \quad u_1 = 0.8865, \quad u_2 = 0.9865.$$

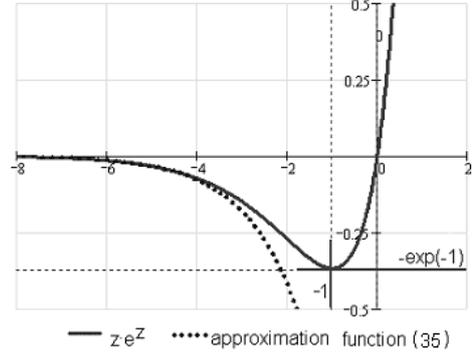


Fig. 3. The method of approximating Lambert W function occurring in the analytical solution for threshold crossing time.

The threshold crossing times for typical interconnect parameters taken from [4] give very good accuracy for the perturbation parameter $\epsilon < 1$. The simulation results compared with SPICE simulation are presented in Section VI.

VI. Simulation results

In this section we present the results for the ramp excitation of single and coupled interconnects.

The example of output voltage signal for the parameters taken from [4] with the rise time $T_r=30\text{ps}$ is presented in Fig. 4. We can see excellent agreement between SPICE and the extended formula (13).

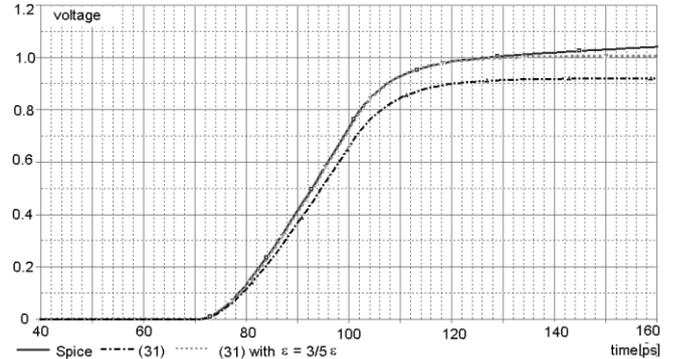


Fig. 4. Ramp response of the single interconnect with parameters taken from [4]. The transmission line model parameters: $R_t=25\Omega$, $L_t=5\text{nH}$, $C_t=1\text{pF}$, $C_0=0.1\text{pF}$, $R_w=25\Omega$, $T_r=30\text{ps}$.

For the coupled interconnects (see the structure in Fig.2) we calculate the RLC transmission line model with the IE3D program and then simulate the output response (13) for the ramp excitation. Fig. 5 present a ramp response of the structure shown in Fig. 2. The transmission line model parameters are: $R_t=84\Omega$, $L_t=8,76\text{nH}$, $C_t=0,3\text{pF}$, $M_t=5,1\text{nH}$, $C_{mt}=76\text{fF}$, $C_0=0.1\text{pF}$ and $R_w=84\Omega$. In this case, after decoupling the lines, one of them has relatively small impedance Z_0 , so the perturbation parameter is close to 1. The

SPICE simulation and approximation with (13) are in good agreement, especially during the first phase of voltage increase.

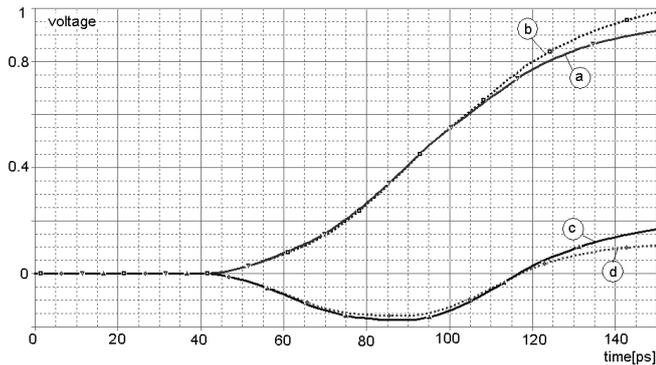


Fig. 5. Ramp response ($T_r=50\text{ps}$) of the coupled interconnects (Fig.2) a) aggressor line obtained from SPICE b) aggressor line computed from (13), c) victim line computed from SPICE, d) victim line computed from (13)

We have simulated some other examples for typical interconnect parameters [4]. The simulations give a relatively small error (with respect to SPICE) for $0 < t < 3T$, both for the ramp and step excitation. Examples of the output voltage signal, presented in Fig. 6 confirms the usefulness of the method for modern interconnects if the condition $\varepsilon < 1$ is satisfied.

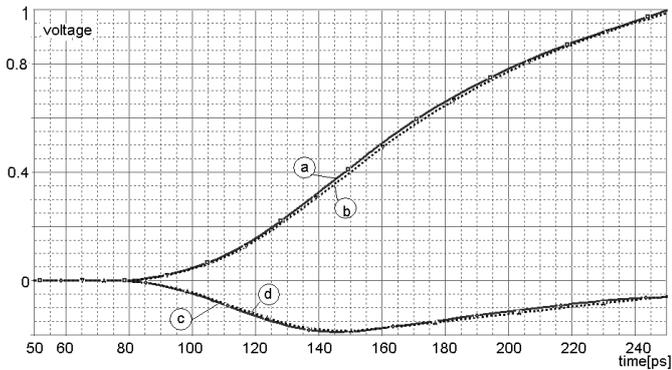


Fig. 6. Ramp response ($T_r=50\text{ps}$) of the coupled interconnects with parameters taken from [4]. The transmission line model parameters: $R_l=25\Omega$, $L_l=8\text{nH}$, $C_l=1\text{pF}$, $M_l=3,2\text{nH}$, $C_{ml}=0.1\text{pF}$, $C_0=1\text{pF}$, $R_w=25\Omega$. a) aggressor line obtained from SPICE b) aggressor line computed from (13), c) victim line computed from SPICE, d) victim line computed from (13)

Conclusions

The presented approach allows computing the signal voltage response ramp signal input. Using the multiple scales method for the low-loss interconnect, we are able to solve the lossless interconnect equation system including the effects of losses in perturbation parameter, to obtain a closed form formula for the ramp response. To obtain the closed form formula for the threshold time we have to approximate the Lambert W function by the logarithmical function, but the approximation does not depend on interconnect parameters. The presented solution for the single interconnect can be easily extended to two coupled interconnects with the same parameters. The comparison with SPICE simulations shows that the presented method is accurate for low-loss interconnects with high inductance.

References

- [1] Deutsch A. et al., "Effects of noise on timing or data-pattern dependent delay variation when transmission-line effects are taken into account for on-chip wiring", Proceedings of the 11th of IEEE Workshop on Signal Propagation On Interconnects, May 2007, Genova, pp. 7-11.
- [2] Ligocka, A. Bandurski, W. "The Low-Loss Interconnect Simulation by Perturbation Methods", Proceedings of the Proceedings of the 11th of IEEE Workshop on Signal Propagation On Interconnects, May 2007, Genova, pp 182-185
- [5] Ligocka A. Bandurski, W. Rydlichowski P. „A New Approach to Analysis and Simulation of Single and Coupled Low-Loss Interconnects.” Proceedings of ECCTD 2007, Sevilla, August 26 - 30, 2007
- [4] Ismail Y.I., Friedman E.G., "Effects of inductance on the propagation delay and repeater insertion in VLSI circuits", IEEE Transactions on VLSI Systems, vol. 8, No. 2, April 2000, pp. 195-206.
- [5] Shivamoggi B.K. "Perturbation methods for differential equations", Birkhauser, Boston 2003.